

IN THE CLAIMS:

Claims 4 and 14 have been cancelled. Claims 22 – 26 have been added.

Claims 1, 6, 7, 11, and 16 – 19 have been amended, as follows:

1. (currently amended) A method of error correction in a high-speed data transmission system, comprising:

determining a value of an input signal at a decision timeframe and holding the value as a tentative value;

estimating an error of the value of the input signal by subtracting the tentative value from the value of the input signal, amplifying the error of the value to create an amplified error, and holding the amplified error of the value as a corrected value to be utilized if the tentative value is to be corrected;

deciding if the amplified error of the value is within a defined marginal range;

determining if the input signal is involved in a transition from a positive to negative state or from a negative to positive state during a symbol period; and

~~correcting~~ selecting the tentative corrected value instead of [[to]] the corrected tentative value to be output if both the amplified error of the value is in the defined marginal range and the input signal is involved in the transition.

2. (original) A method of error correction in <sup>the</sup> ~~a~~ high-speed data transmission system according to claim 1, wherein two adjacent values of the input signal are calculated before and after the decision timeframe to determine if the input signal is involved in <sup>the</sup> ~~a~~ transition.

3. (original) A method of error correction in <sup>the</sup> a high-speed data transmission system according to claim 2, wherein the two adjacent values are calculated one-half a symbol period before and after the decision timeframe.

Claim 4 (cancelled).

5. (original) A method of error correction in <sup>the</sup> a high-speed data transmission system according to claim 3, wherein the two adjacent values are involved in a transition from  $-1$  to  $+1$ , or from  $+1$  to  $-1$ .

6. (currently amended) A decision system in high-speed data transmission, comprising:

a data decision circuit to determine a value of an input signal at a decision instance and to hold the value of the input signal as a tentative value;

an error estimator module to determine an error value of the value of the input signal by subtracting the tentative value from the value of the input signal, to amplify the error value to create an amplified error of the value, and to hold the amplified error value as a corrected value to be utilized if the tentative value is to be corrected;

an error verifier module to determine whether the amplified error value is within a marginal range;

a transition detecting module, to determine whether the input signal was in transition from a positive to negative state, or a negative to positive state during a symbol period; and

an error correction module to determine whether the tentative value should be overridden by the corrected value if both the amplified error of the value is within the marginal range and the input signal is involved in the transition.

7. (currently amended) ~~The decision system according to claim 6,~~ A decision system for utilization in high-speed data transmission, comprising:

a data decision circuit to determine a value of an input signal at a decision instance and to hold the value of the input signal as a tentative value;

an error estimator module to determine an error value of the value by subtracting the tentative value from the value of the input signal, to amplify the error value to created an amplified error value, and to hold the amplified error value as a corrected value to be utilized if the tentative value needs to be corrected;

an error verifier module to determine whether the amplified error value is within a marginal range;

a transition detecting module, to determine whether the input signal was in a transition from a positive to negative state, or a negative to positive state during a symbol period; and

an error correction module to select the corrected value instead of the tentative value if the error verifier module determines the amplified error value is outside the marginal range and the transition detecting module determines that the input signal was <sup>the</sup> in transition.

wherein the error verifier module includes an absolute value circuit to make the <sup>amplified</sup> error value a positive number and a comparator to compare the <sup>positive number</sup> error value to a reference value.

8. (original) The decision system according to claim 6, wherein adjacent sample values of the input signal before and after the decision instance are used to determine if the input signal is <sup>the</sup> in transition.

9. (original) The decision system according to claim 8, wherein the adjacent <sup>sample</sup>~~samples~~ values are calculated one-half a symbol period before and after the decision instance.

10. (original) The decision system according to claim 8, wherein the transition detecting module includes an adder to add the adjacent sample values, an absolute value circuit to make positive the added adjacent sample values, and a comparator to compare the added adjacent sample values to a reference value.

11. (currently amended) A receiver utilized in high speed data transmission to output data values, comprising:

an analog-to-digital converter to receive an input signal and to output a sampled digital signal and a phase information; and

a decision system to receive the sampled digital signal and to output a value from the receiver, wherein the decision system:

receives the sampled digital signal, calculates a value at a decision instance, and assigns a tentative value;

calculates an error value of the input signal by subtracting the tentative value from the value of the input signal, amplifies the error value to create an amplified error of the value, and holds [[it]] the amplified error of the value as a corrected value to be utilized if the tentative value is to be corrected;

determines if the error value is within a marginal range;

determines whether the input signal was in a transition from a positive to negative state, or a negative to positive state during a symbol period; and

outputs the corrected value ~~as the value~~ instead of the tentative value if the amplified error value is within the marginal range and if the input signal is in ~~[[a]]~~ the transition during ~~a~~<sup>the</sup> symbol period~~[[;]]~~ .

~~a phase detector to receive the value and the phase information and to output a detected phase information;~~

~~a loop filter to receive the detected phase information and to output a filtered phase information; and~~

~~an oscillator to receive the filtered phase information and to output a clock signal as a sampling clock for the analog-to-digital converter.~~

12. (original) The receiver according to claim 11, wherein adjacent sample values of the input signal before and after the decision instance are used to determine if the sampled digital signal is within ~~a~~<sup>the</sup> transition.

13. (original) The receiver according to claim 12, wherein the adjacent sample values are calculated one-half a symbol period before and after the decision instance.

Claim 14 (cancelled).

15. (currently amended) ~~The receiver according to claim 14,~~ A receiver utilized in high speed data transmission to output data values, comprising:

an analog-to-digital converter to receive an input signal and to output a sampled digital signal and phase information; and

a decision system to receive the sampled digital signal and to output a corrected value from the receiver, the decision system including,

a data decision circuit to determine a value of the sampled digital signal at a decision instance and to hold the value of the sampled digital signal as a tentative value;

an error estimator module to determine an error value of the value of the sampled digital signal by subtracting the tentative value from the value of the sampled digital signal, to amplify the error value to create an amplified error value, and to hold the amplified error value as the corrected value to be utilized if the tentative value needs to be corrected;

an error verifier module to determine whether the amplified error value is within a marginal range;

a transition detecting module, to determine whether the sampled <sup>digital</sup> signal was in a transition from a positive to negative state, or a negative to positive state during a symbol period; and

an error correction module to select the corrected value instead of the tentative value if the error verifier module determines the amplified error value is outside the marginal range and the transition detecting module determines that the input signal was <sup>the</sup> in transition,

wherein the error verifier module includes an absolute value circuit to make the <sup>amplified</sup> error value a positive number and a comparator to compare the <sup>positive number</sup> error value to a reference value.

16. (currently amended) The receiver according to claim <sup>15</sup> ~~11~~, wherein the transition detecting module includes an adder to add the adjacent sample values, an

absolute value circuit to make positive the added adjacent sample values, and a comparator to compare the added adjacent sample values to a reference value.

17. (currently amended) The [[system]] receiver according to claim 11, wherein the input signal is received from a T1 data transmission system.

18. (currently amended) The [[system]] receiver according to claim 17, wherein the T1 data transmission system includes a plurality of cascaded T1 links.

19. (currently amended) A decision circuit, comprising:

a machine-readable storage medium; and

machine-readable program code, stored on the machine readable storage medium, the machine-readable program code having instructions, which when executed, cause the <sup>decision</sup> circuit to

calculate a value of an input signal at a decision instance and to hold the value as a tentative value,

calculate an error value of the input signal by subtracting the tentative value from the value of the input signal, amplify the error value to create an amplified error value, and hold the amplified error value as a corrected value to be utilized if the tentative value is to be corrected,

determine whether the amplified error value is within a marginal range,

determine whether the input signal was in <sup>a</sup> transition from a positive to negative state, or from a negative to positive state during a symbol period, and

decide whether the tentative value should be overridden by the corrected value if both the amplified error of the value is in the defined marginal range and the input signal is involved in the transition.

20. (original) The decision circuit according to claim 19, wherein adjacent samples of the input signal before and after the decision instance are used to determine if the input signal is in <sup>the</sup> transition.

21. (original) The decision circuit according to claim 20, wherein the adjacent sample values of the input signal are calculated one-half a symbol period before and after the decision instance.

22. (new) The method of claim 1, wherein <sup>said</sup> amplifying the error of the value to create <sup>the</sup> an amplified error includes sending the error of the value through a signed Boolean circuit to amplify all negative values to -1 and to amplify all positive values to +1.

23. (new) The method of claim 1, wherein <sup>said</sup> deciding if the amplified error of the value is within <sup>the</sup> a defined marginal range utilizes an absolute value circuit making the amplified error <sup>of the</sup> value a positive number and a comparator to compare the <sup>positive number</sup> error value to a reference value.

24. (new) The receiver of claim 11, further including a phase detector to receive the value and the phase information and to output a detected phase information.

25. (new) The receiver of claim 24, further including a loop filter to receive the detected phase information and to output filtered phase information.

26. (new) The receiver of claim 25, further including an oscillator to receive the filtered phase information and to output a clock signal as a sampling clock for the analog-to-digital converter.